Gil VINITZKY

SERIAL NO.:

09/586,775

FILED:

June 5, 2000

Page 5

Remarks:

The present response is intended to be fully responsive to all points raised by the Examiner and is believed to place the application in condition for allowance. Allowance of the application is respectfully requested.

Status of Claims

Claims 1-8 are pending in the application. Claims 3-5, 7 and 8 are objected to. Claims 1-8 are rejected. Claims 3 and 5 have been amended, and claims 7 and 8 have been cancelled without prejudice. Applicants respectfully submit that the amendments to claims 3 and 5 do not add new matter.

Claim Objections

Claims 3-5, 7 and 8 are objected to for not disclosing the use of the method recited in the preamble. Claims 7 and 8 have been cancelled without prejudice, thus rendering the objection moot. Claims 3 and 5 have been amended to recite "A method for in-place memory management for Fast Fourier Transform calculations", thus curing the objection.

Claim Rejections - 35 USC 112

Claims 7 and 8 are rejected under 35 USC 112, second paragraph for lack of antecedent basis for "the sum". Claims 7 and 8 have been cancelled without prejudice, thus rendering the rejection moot.

Claim Rejections - 35 USC 102

Claims 7 and 8 are rejected under 35 USC 102(b) as being anticipated by US Patent No. 3,673,399 (Hancke et al.). Claims 7 and 8 have been cancelled without prejudice, thus rendering the rejection moot.

Claim Rejections - 35 USC 103

Claims 1-6 are rejected under 35 USC 103(a) as being unpatentable over Hancke et al. in view of US Patent No. 3,871,577 (Avellar et al.). Applicant respectfully traverses this rejection, in view of the remarks that follow.

Claims 1 and 2

In the "Response to Arguments", the Examiner wrote that the Applicants arguments in the response to the previous Office Action are not persuasive.

Gil VINITZKY

SERIAL NO.:

09/586,775

FILED: Page 6

June 5, 2000

As discussed in the response to the previous Office Action, the teaching of Hancke et al. is that for Pass 1 (the equivalent of FFT stage 0), the data points (operands) are read from input buffer memory 60 (Fig. 6), which is part of input buffer 23 (Fig. 1), and the results are stored buffer 24 and buffer 25, not at the memory address from which the operands were

fetched.

In the response to the previous Office Action, Applicants argued that in Avellar et al., the output of the first pass is stored in different memories than the input buffers. In this Office Action, the Examiner responded that "Avellar et al.'s Figure 1 only discloses two memory banks (101 and 102) for storing input and output of FFT data".

Applicants respectfully submit that this is incorrect. Figure 1 of Avellar et al. discloses six memory banks: 10, 12, 16, 18, 20 and 22. In Pass 1, memory banks 10 and 12 store the input and memory banks 16 and 18 store the output. (col. 3, lines 36-63)

Accordingly, Hancke et al. and Avellar et al., alone and in combination, fail to teach or suggest all the limitations of claim 1. Claim 2 is dependent from claim 1 and includes all the limitations of the independent claim. Consequently, the Office Action has failed to establish a *prima facie* case of obviousness for claims 1 and 2.

Claims 3 - 6

The Examiner has rejected claims 3 and 5 under the same rationale of rejected claim 1, and has rejected claim 6 under the same rationale of rejected claim 5.

The Examiner has rejected claim 4 under the same rationale of rejected claim 2.

Applicants have presented remarks above explaining why Hancke et al. and Avellar et al., alone and in combination, fail to teach or suggest all the limitations of claim 1 or claim 2. Accordingly, Hancke et al. and Avellar et al., alone and in combination, fail to teach or suggest all the limitations of claims 3-6.

In particular, Hancke et al. and Avellar et al., alone and in combination, fail to teach or suggest the following limitation of claim 3: "storing a first output data point of said initial stage at said first address in said first memory space and a second output data point of said initial stage at said second address" where "said first address" refers to the address in the first memory space "where a first data point of a pair of input data points of an initial stage

Gil VINITZKY

SERIAL NO.:

09/586,775

FILED:

June 5, 2000 Page 7

of a Fast Fourier Transform calculation is stored" and "said second address" refers to the address in the second memory space "where a second data point of said is stored".

Furthermore, Hancke et al. and Avellar et al., alone and in combination, fail to teach or suggest the following limitation of claim 5: "determining ... whether to store an output data point of an initial stage of a Fast Fourier Transform calculation in a first memory space at a first address or in a second memory space at a second address, where a first data point of a pair of input data points of said initial stage is stored in said first memory space at said first address and a second data point of said pair is stored in said second memory space at said second address, and where said first address and said second address both correspond to said memory index".

Moreover, Hancke et al. and Avellar et al., alone and in combination, fail to teach or suggest the following limitation of claim 6: "means for determining ... whether to store an output data point of said initial stage in said first memory space at said first address or in said second memory space at said second address", where "said first address" refers to the address in the first memory space where "a first data point of a pair of input data points of an initial stage" are stored and where "said second address" refers to the address in the second memory space where "a second data point of said pair" are stored.

Consequently, the Office Action has failed to establish a prima facie case of obviousness for claims 3 - 6.

35 USC 132

The Examiner has stated that claims 7 and 8 include new matter, specifically the limitation "the first/second address that is sum of a first/second base address and memory index" is not supported by the original specification.

Claims 7 and 8 have been cancelled, thus rendering this issue moot.

Gil VINITZKY 09/586,775

SERIAL NO.: FILED:

June 5, 2000

Page 8

Should the Examiner have any question or comment as to the form, content or entry of this Amendment, the Examiner is requested to contact the undersigned at the telephone number below. Similarly, if there are any further issues yet to be resolved to advance the prosecution of this application to issue, the Examiner is requested to telephone the undersigned counsel.

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espectfully submitted,

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